AMTC Letters
Vol. 1 (2008)
© 2008 Japan Fine Ceramics Center

C_s-corrected TEM/STEM Analysis of La_2O_3/Si (001)

Shin Inamoto[1], Jun Yamasaki[2], Eiji Okunishi[3], Kuniyuki Kakushima[4], Hiroshi Iwai[5], Nobuo Tanaka[2]

[1]Department of Crystalline Materials Science, Nagoya University, Nagoya 464-8603, Japan
[2]EcoTopia Science Institute, Nagoya University, Nagoya 464-8603, Japan
[3]JEOL Ltd., Akishima 196-8558, Japan
[4]Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Yokohama 226-8503, Japan
[5]Frontier Research Center, Tokyo Institute of Technology, Yokohama 226-8503, Japan

In recent years, reduction of thickness of gate dielectric in metal-oxide-semiconductor field effect transistors (MOSFETs) leads to increase in gate leakage current, which becomes a serious problem [1]. In order to overcome this problem, researches and developments to change the gate dielectrics from SiO_2 to other materials having high dielectric constants, so-called, high-k materials have been actively performed [2-5]. Among various high-k materials, La_2O_3 is considered as one of the candidates for the future gate dielectrics. In this study we have analyzed annealing behavior of thickness, and elemental composition of thin layers and surficial/interfacial roughness in La_2O_3/Si(001) by using spherical aberration (C_s) -corrected electron microscopes.

After removing an oxidized layer on a Si(001) substrate, a La_2O_3 film 4nm in thickness is deposited on the substrate at room temperature by electron-beam evaporation, and then post deposition annealing (PDA) is performed for 5 min at 300 or 500 ℃ in N_2 atmosphere. All samples, i.e. the as-deposited and the 300 ℃ / 500℃ PDA samples, are thinned for cross-sectional observations by the standard method using ion-milling after mechanical dimpling. Transmission electron microscope (TEM) / high-angle annular dark-field scanning transmission electron microscope (HAADF-STEM) observations and electron energy loss spectroscopy (EELS) measurements are performed by using JEM-2100F equipped with C_s-correctors for the illumination system and the imaging system.

Figures 1(a) and (b) show TEM and HAADF-STEM images of the La_2O_3/Si interface after the 300 ℃ PDA, respectively. The bilayer structures of Si-oxide and La-silicate seen in Figures 1(a) and (b) are formed in all the samples. The results of measuring surficial and interfacial roughness indicate that they increase rapidly after the 500 ℃ PDA. It is considered that the increase is the reason of the higher channel mobility after the 300 ℃ PDA than after the 500 ℃ PDA in electrical measurements[2]. Thickness of each layer has been also measured from the images in careful consideration of superposition of projected interfacial roughness. Figure 2 shows elemental profiles across the gate stack measured by EELS. It turns out that the composition ratio of oxygen atoms in the La-silicate layer increases by about 1.6 times after the PDAs, and the ratio of lanthanum atoms increases by about 1.2 times after the 500 ℃ PDA, respectively. From all the above results, an atomic diffusion model during the PDAs is proposed as follows. During the 300 ℃ PDA, the number of oxygen defects contained in the as-deposited films decreases and La-Si bonds change to La-O-Si bonds as the result of absorbing residual oxygen in the N_2 atmosphere. During the 500 ℃ PDA, La-Si bonds change to La-O-Si bonds as well. In addition, as the result of thermal diffusion of lanthanum atoms in the La-silicate film, a part of La-O-Si bonds changes to La-O-La bonds. These changes are considered to be another reason for the highest channel mobility after the 300 ℃ PDA, because the mobility is suppressed by electric dipoles of La-Si and La-O-La bonds.

In summary, we have found out the reasons for the degradation of the gate mobility after the 500 ℃ PDA, and have elucidated the atomic diffusion mechanism during the PDAs [6]. It is expected that these results provide important information for producing devices with higher performance.

References

[1] S. H. Lo, et al., IEEE Electron Device Lett. **18** (1997) 209

© 2008 Japan Fine Ceramics Center

[2] J. A. Ng, et al., Microelectron. Eng. **80** (2005) 206
[3] G. D. Wilk, et al., J. Appl. Phys. **89** (2001) 5243
[4] P. D. Kirsch, et.al., J. Appl. Phys. **91** (2002) 4353
[5] A. Chin, et al., Tech. Dig. VLSI Symp. (2000) 16
[6] S. Inamoto, et al., in preparation.

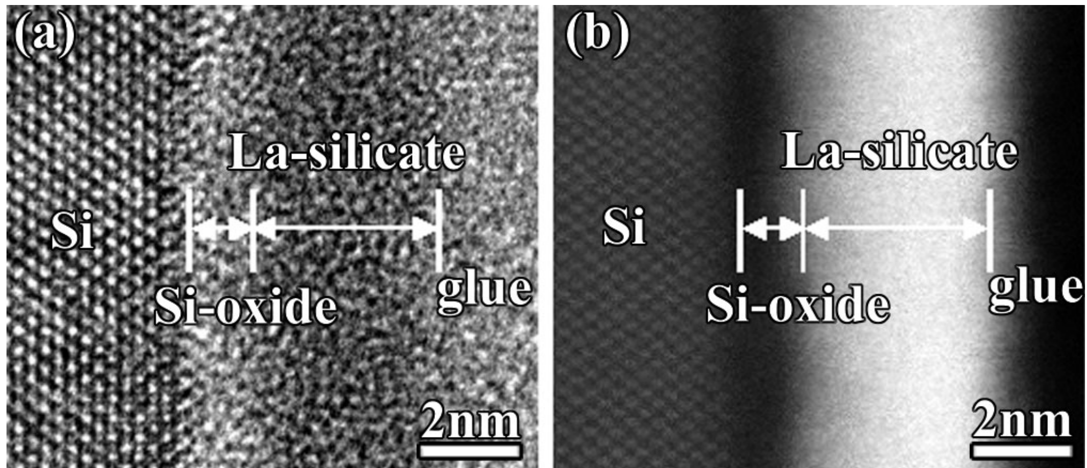

FIG. 1. Cross-sectional observations of the La_2O_3/Si interface.
(a) C_s-corrected TEM image, (b) C_s-corrected HAADF-STEM image.

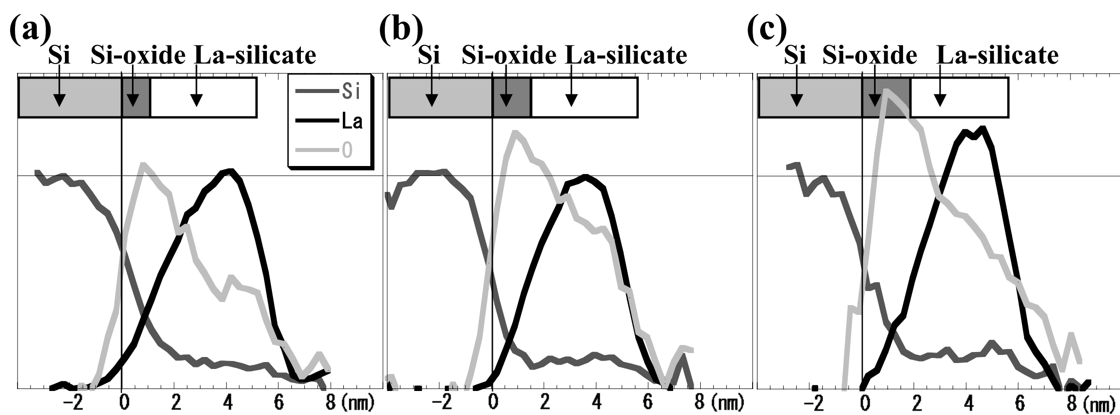

FIG. 2. Elemental profiles across the gate stacks measured by EELS.
(a) As-deposited, (b) 300℃ PDA, and (c) 500℃ PDA samples.