# *Ab-initio* study of metal/oxide interfaces under bias voltage utilizing the orbital separation approach

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As the scaling trend of nanoelectronics devices continues towards single digits in the nanometer regime, it is beginning to be recognized that the properties of interfaces can seriously affect the performance of devices. For example, the interface of very-high-k oxides such as $SrTiO_3$ or $TiO_2$ and metal often suffer from degraded dielectric properties due to, e.g., contamination, defects, and the intrinsic dead layer effect [1, 2]. This results in the capacitance of metal/high-k oxide/metal capacitors being much smaller than expected from the bulk dielectric constant, and poses a problem for further scaling of dynamic random access memory devices. In this work, we develop a new first principles technique based on the Kohn-Sham method that we call "orbital separation approach" [3]. Using this method, we examine the dielectric response of metal/insulator interfaces under bias voltage. We also calculate the capacitance at various dielectric thicknesses and discuss the effect of the interface on the capacitance values.

The orbital separation approach was implemented in the VASP code. We performed relaxation of Au/MgO/Au and $SrRuO_3$/$SrTiO_3$/$SrRuO_3$ (SRO/STO/SRO) slabs with bias voltage applied on the two electrodes. The interfaces in both models are epitaxial in the (100) orientation. The capacitance values were calculated from the variation of the total energy with respect to bias voltage ($C = 1/V\, \mathrm{d}E/\mathrm{d}V$).

Figures 1 and 2 show the change in the electrostatic potential due to bias application in the Au/MgO/Au and SRO/STO/SRO systems, respectively. The potential drops almost linearly inside MgO. On the other hand, the potential drops acutely at the SRO/STO interface rather than being linear through the entire insulator. This means that the dielectric constant at the interface is reduced from the bulk value. This was also reported in a previous work, and is called the intrinsic dead layer [2]. Figure 3 shows the calculated inverse capacitance of the capacitors with respect to thickness. It is seen that the inverse capacitance for SRO/STO/SRO capacitor is mostly linear with respect to thickness, but interpolation to zero thickness does not go through the origin. This means that the capacitance is decreased due to the dead-layer effect, which occurs even for perfectly epitaxial interfaces. The effect is not clearly seen for the MgO capacitor, presumably due to the much lower bulk dielectric constant of MgO.

References

[1] C. S. Hwang, J. Appl. Phys. 92 (2002) 432.
[2] M. Stengel and N. Spaldin, Nature 443 (2006) 679.
[3] S. Kasamatsu et al., Phys. Rev. B 84 (2011) 085120.

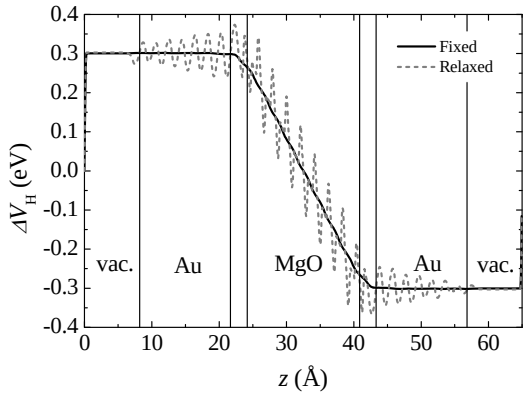


FIG. 1. Change of electrostatic potential due to bias application in the Au/MgO/Au system. The results are given for when the atomic positions are fixed (solid line) or relaxed (dashed line) at 0.6 V.

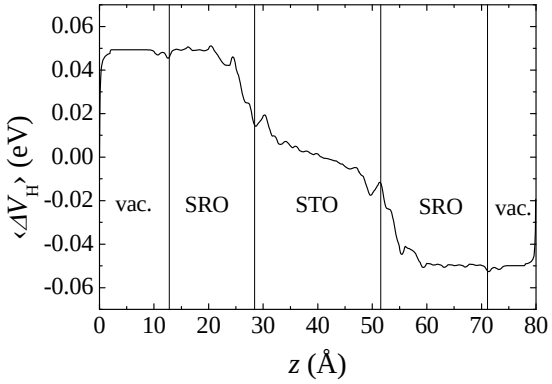


FIG. 2. Change in the electrostatic potential due to bias application in the SrRuO3/SrTiO3/SrRuO3 system. The result is given for when the structure was relaxed at 0.1 V. Atomic level oscillations are smoothened using macroscopic averaging.

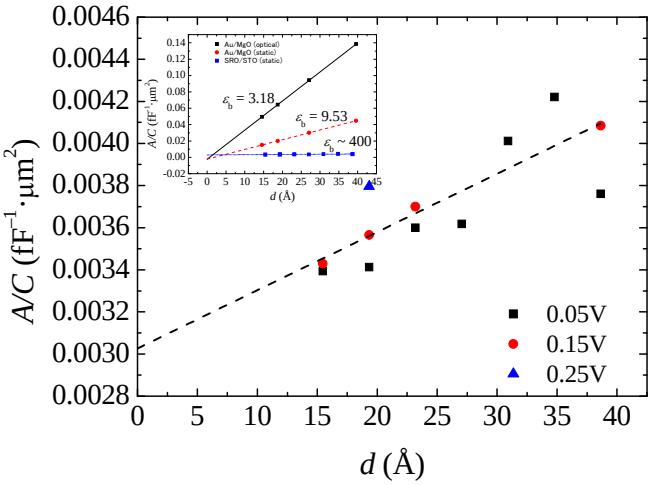


FIG. 3. The inverse capacitance of the SRO/STO/SRO capacitor with respect to STO thickness calculated at various bias voltages. Inset: Comparison with MgO.